## EE272B Project Proposal: Current Mode Buck Converter with Digital Monitoring

## (The Open PMIC Project)

## Application

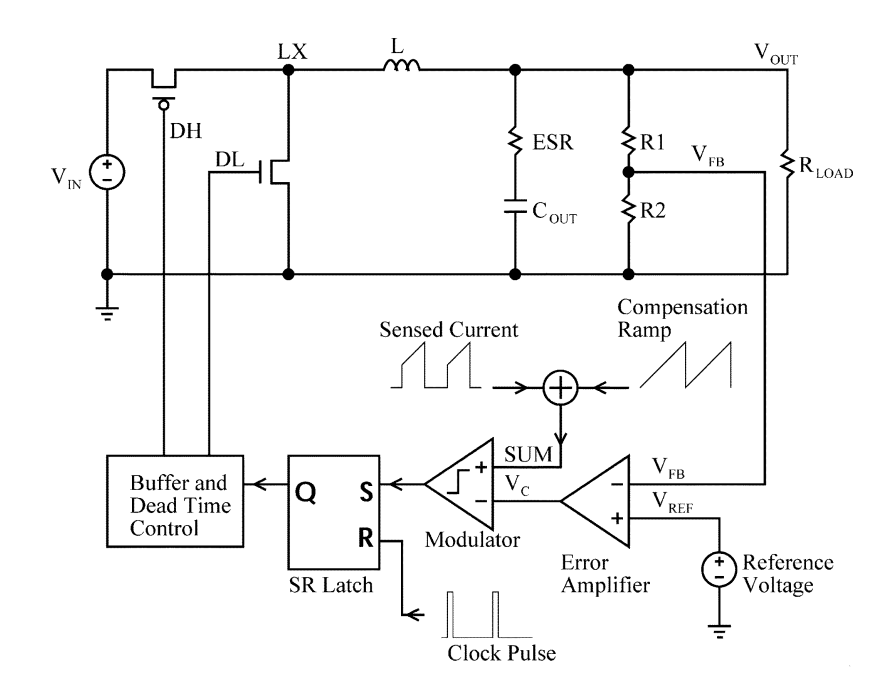
For embedded systems a supply voltage of 3V3 is common due to I/O standards, despite the fact that digital logic can run at lower supply voltages with reduced power consumption. Many commercial microcontrollers have separate supply pins for I/O and digital logic, allowing for separate supply voltages and a lower total power usage, but many times this feature is not used due to the added BOM cost and circuit complexity.

Some commercial microcontrollers have the circuitry for a buck converter on die, only requiring an external inductor and a few capacitors to generate the lower voltage supply rail. The goal of this project is to produce open source IP for a similar embedded buck converter that can be used in other designs, such as SoCs, on the sky130 process node. The buck converter will generate a 1V8 supply rail for the digital logic from a 3V3 supply rail.

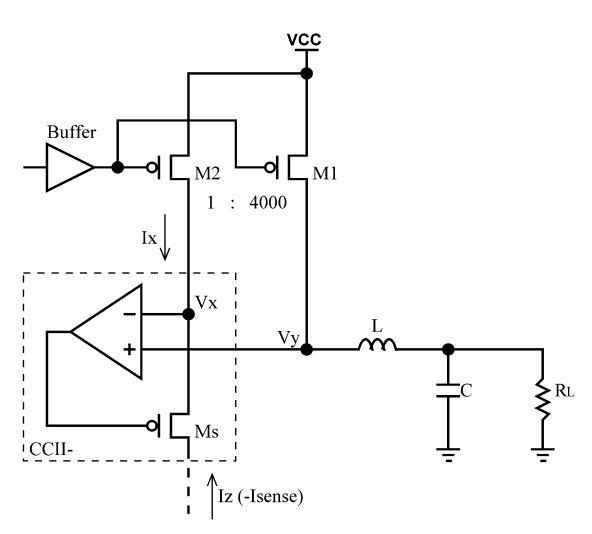
The nominal output power will be determined by the available die area and the sizing of the PFET and NFET in the power stage, but is tentatively 300mA at 1.8V, which is 0.5W and should be sufficient to a wide range of projects on the SKY130 process node.

## Related Work

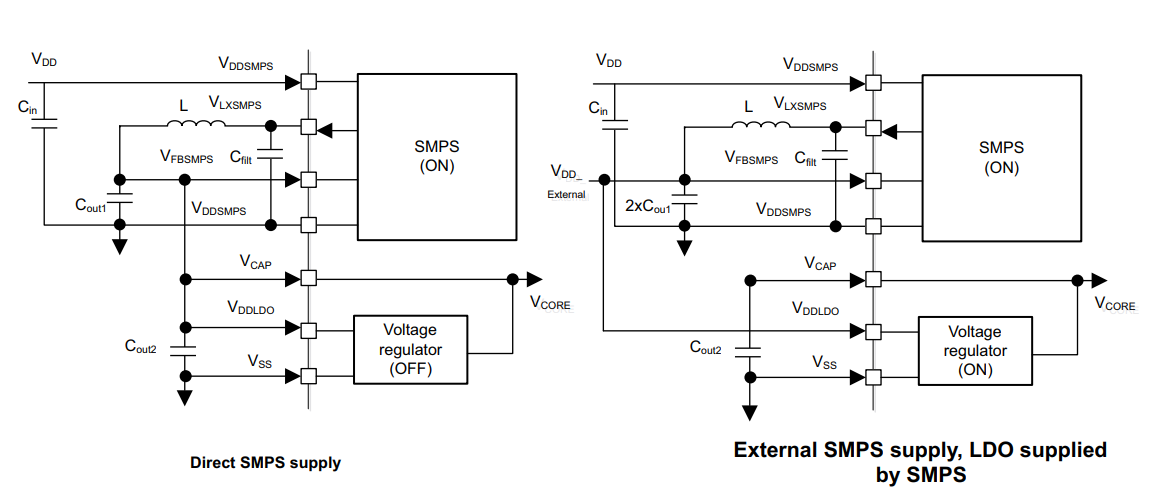
The implemented converter will be a buck converter using peak current mode control[1]. A simplified schematic diagram of a peak current mode control buck converter from [2] is shown below. In peak current mode control the error voltage between the output voltage and reference voltage is used to control the peak inductor current instead of the duty cycle as in a normal buck converter. This provides faster transient response as well as improved protection of the switching devices from over-current.



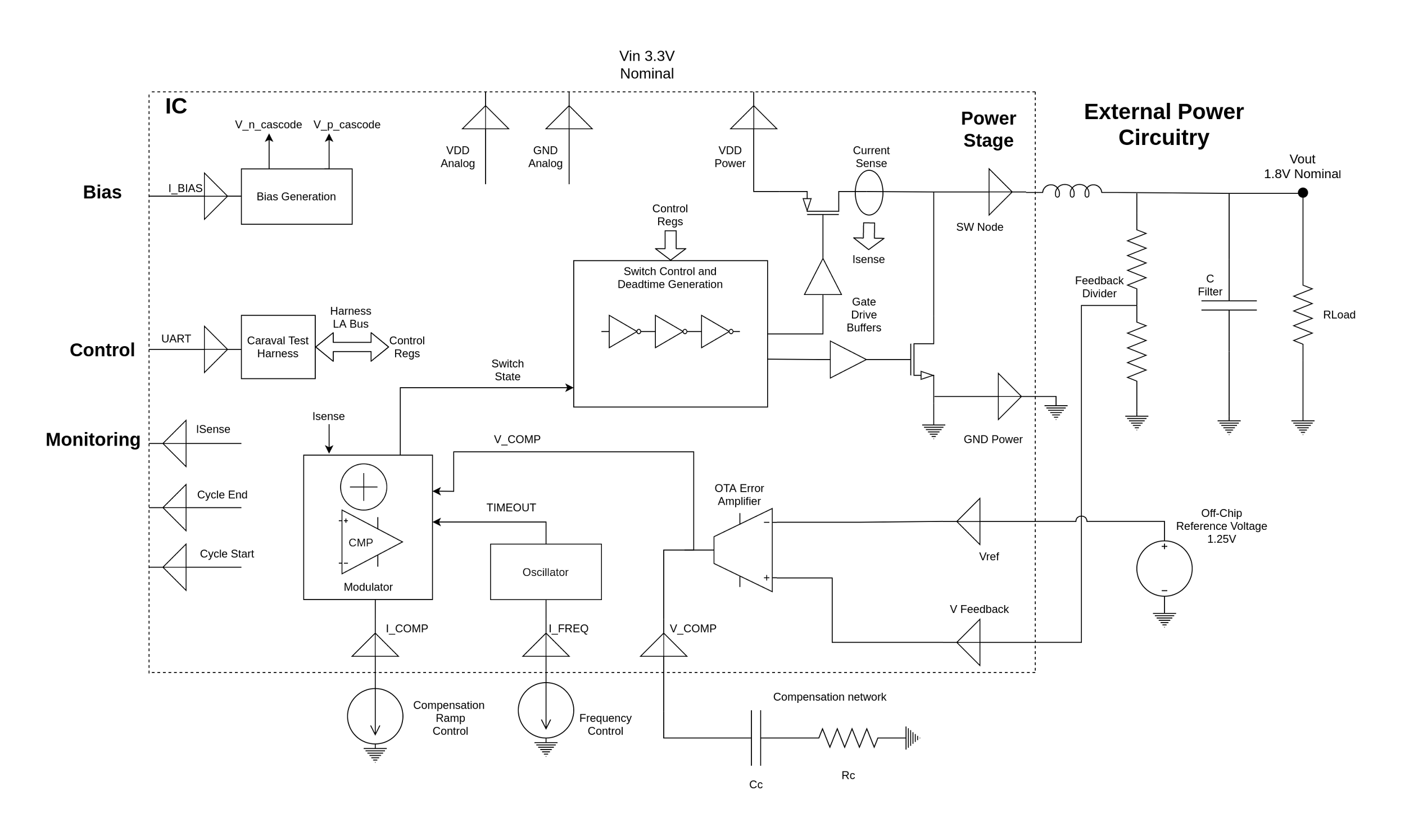
While current sensing adds complexity in discrete power converters it is relatively easy to implement in ASICs with ratiometrically sized FETs [2,3]. Below we show a schematic copied from [2] showing one such current sensing scheme.



At a functional level our goal is to design something similar to the DC/DC converters integrated into modern SOCs. One such example is the buck converter in the STM32F725. We present a block diagram copied from that chips datasheet below[4].



## Approach buck converter



The project is largely a system level design, comprising a number of discrete building blocks which can be largely designed and simulated independently. The converter will have an analog control loop and a digital monitoring and adjustment system which will allow for monitoring of voltage excursions, minor adjustment of the output voltage, and trimming of operating parameters such as dead time for testing and bringup. The output voltage monitoring and adjustment will roughly copy what would be required to implement dynamic voltage scaling, but, lacking an actual processor, our ASIC will not actually implement dynamic voltage scaling.

Our architecture is based on the designs of [2] and [3]. Below we present a block diagram of our system with the external support circuitry shown and I/O pins marked as well as a table of target specifications. To reduce design risk and to make testing the ASIC easier the compensation network, voltage reference, and adjustment for the operating frequency control, are all implemented off chip.

| Vin | 3.3V +- 25% |
| --- | --- |
| Vout | 1.8V |
| Iout,max | 300mA |
| Switching Frequency | 300Khz |
| Efficiency (target) | 85% |

If the timeline is constrained the output voltage monitoring and vref adjustment can be removed.

# Major Tasks

Here we break down the design into the major design blocks, which can be tested independently. These blocks reuse two functional units, a folded cascode opamp and a comparator. This reuse should reduce design risk and reduce design work.

### OTA error amplifier

The error amplifier is based on an operational transconductance amplifier. It can be implemented as a folded cascode opamp, which is one of our functional units. A common reference voltage is 1.25V, which is generated by a bandgap voltage reference. However, this voltage is just at the edge of the input common mode voltage range for the folded cascode opamp, so we instead use a 1.5V reference voltage.

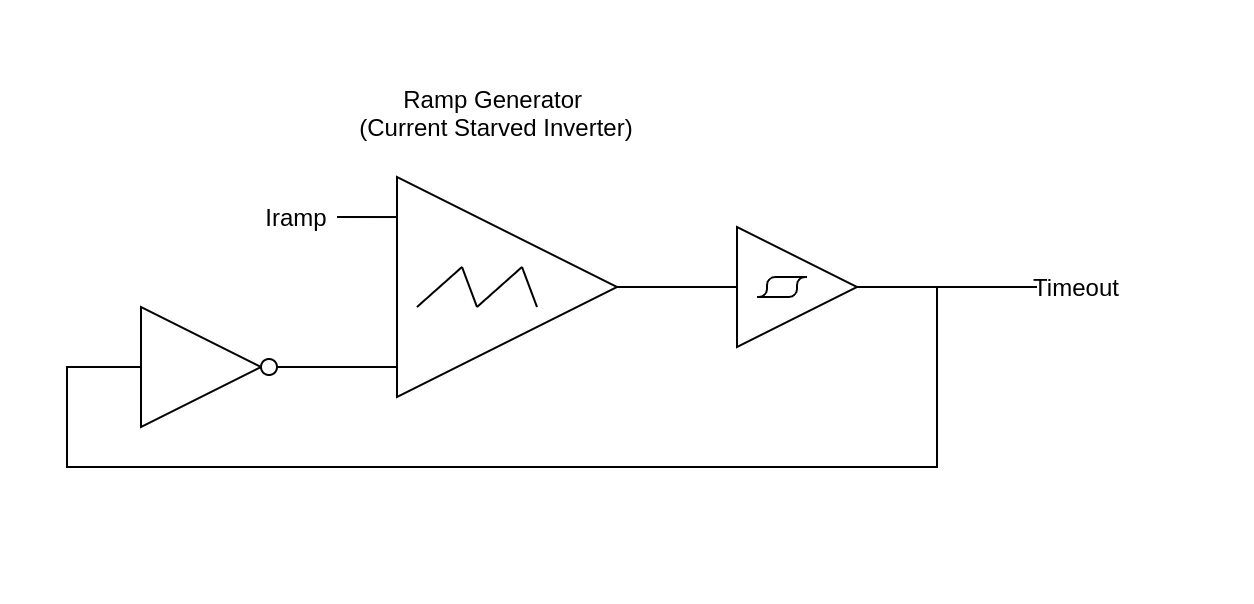
### Oscillator

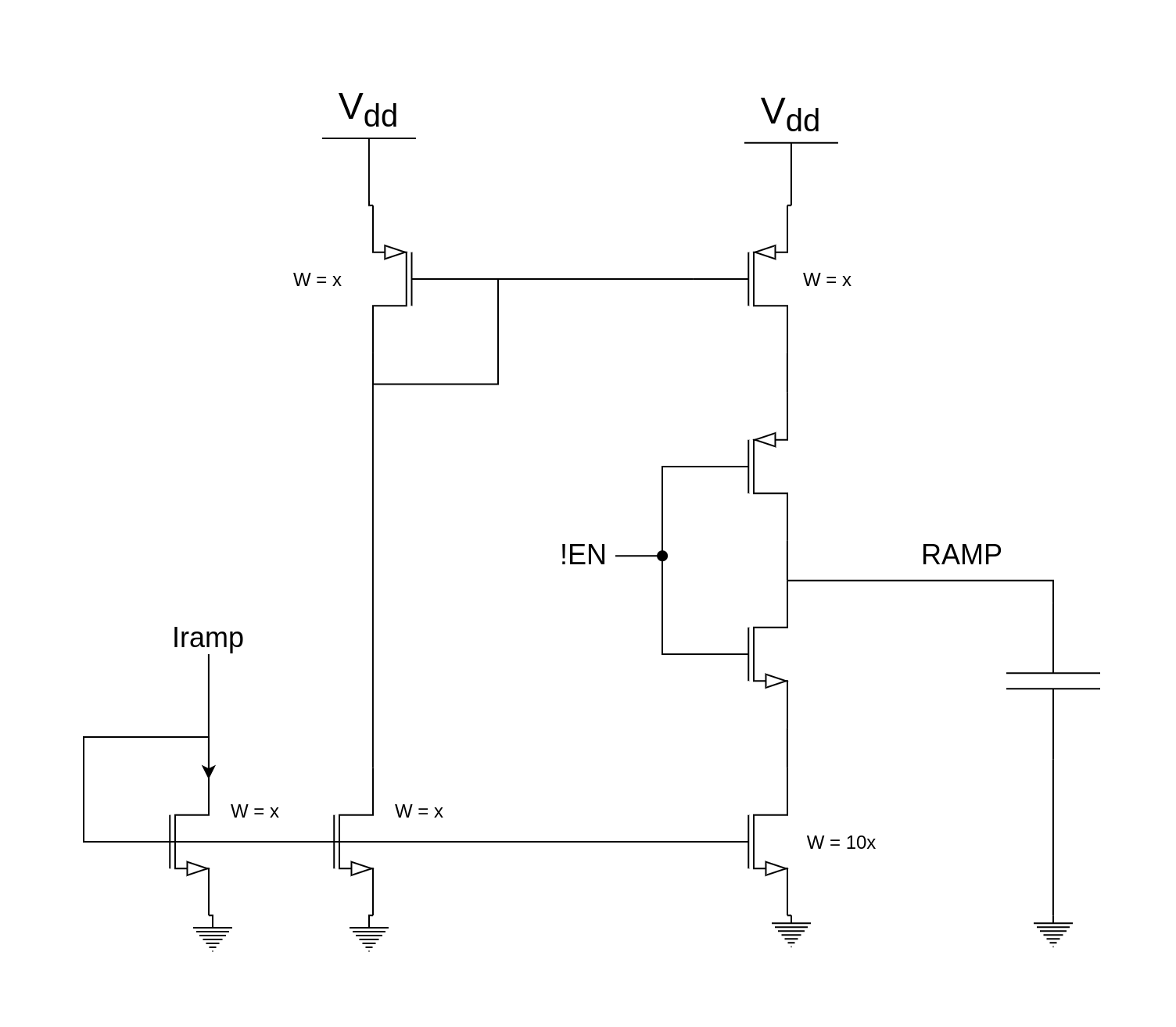
This block generates a timeout pulse with adjustable frequency. This pulse is used to start the switching cycle and is also used to blank the current sense circuity for a period after the start of the switching cycle to prevent false triggering due to switching noise.

This oscillator is implemented as a current starved inverter feeding an on-die capacitor and a schmitt trigger. By adjusting the bias current (supplied from off chip) the frequency can be adjusted. By sizing the P and N stage bias currents relative to another the relative rise and fall rate of the ramp can be adjusted, allowing for adjustment of the duty cycle to ensure that the timeout pulse is long enough to provide sufficient blanking. [6] provides implementation details related to such a configuration.

This circuit requires some logic gates, which can be provided by the SKY130 sky130\_fd\_sc\_hvl - High Voltage (5V) logic library.

Below is a block diagram of the oscillator and a schematic of the current starved inverter with example FET sizing.





### Modulator and Slope Compensation

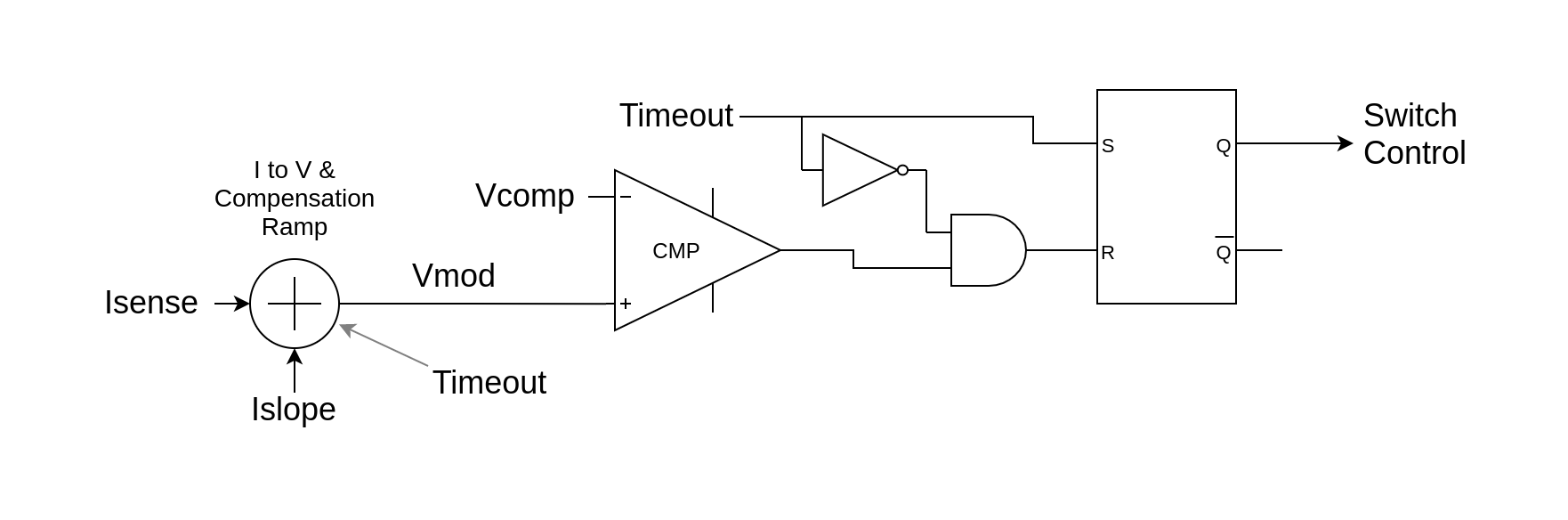
The modulator compares the sensed current signal to the voltage generated by the error amplifier, terminating the switching cycle when the current rises above the setpoint. This utilizes a comparator, which is one of our functional units. Due to the blanking of the current signal at the start of each switching cycle and the amplitude of the current signal, the comparator can use significant hysteresis.

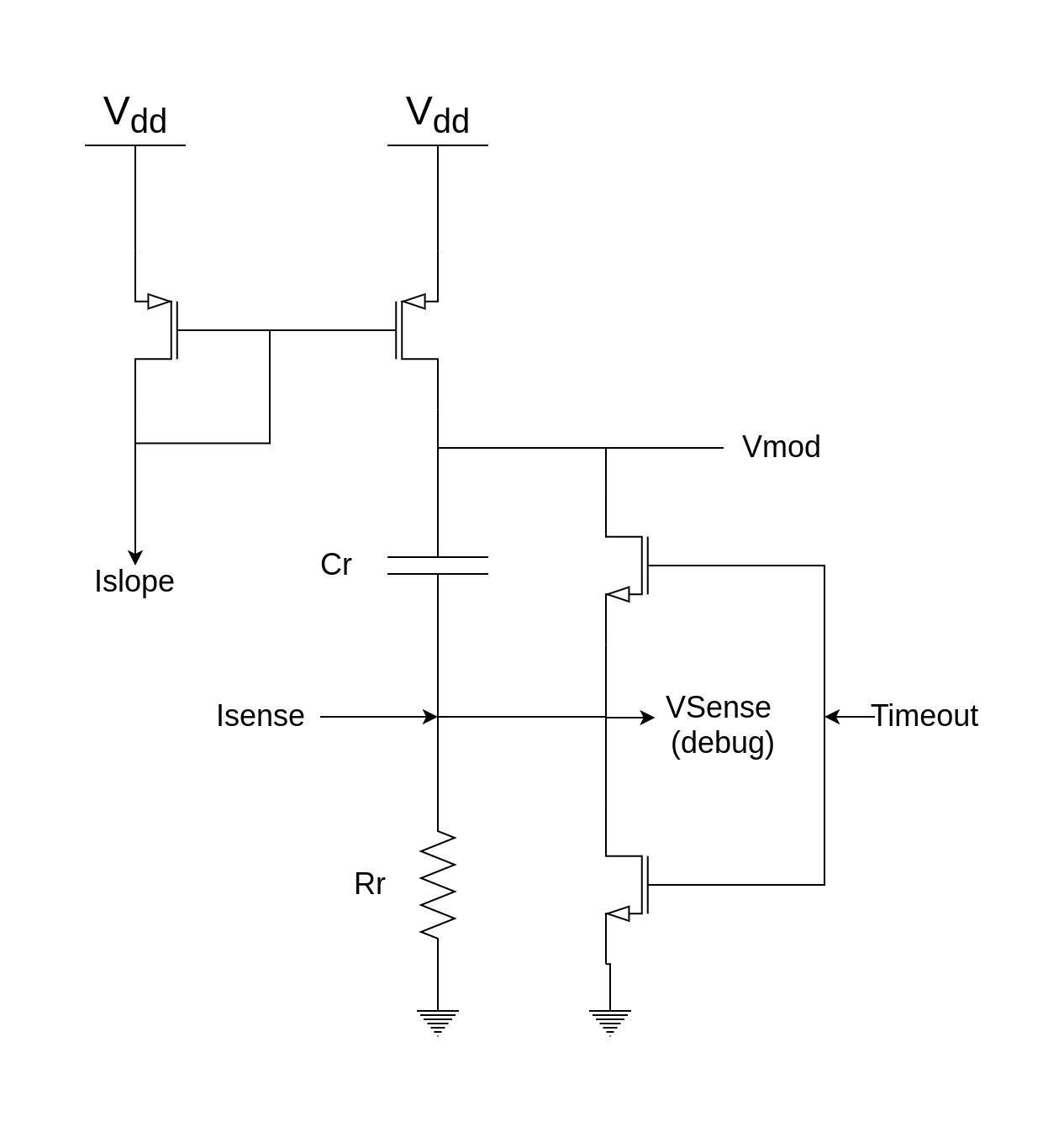
In order to prevent sub-harmonic oscillation of the buck converter, slope compensation is required, which involves adding a reference ramp to the current signal [1].

[2] provides a novel circuit for slope compensation that we plan to use. This circuit performs the current to voltage conversion for the sensed inductor current, allows for the compensation slope to be externally set, and provides a way to blank the current signal during the switching transition, preventing false triggering due to noise.

The timeout signal generated by the oscillator both resets the SR latch used to control the switching state and resets the compensation ramp. The pulse width of the timeout signal sets the blanking period and determines a minimum duty cycle for the converter.

Below we show a block diagram of the modulator and a schematic of the slope compensation scheme.



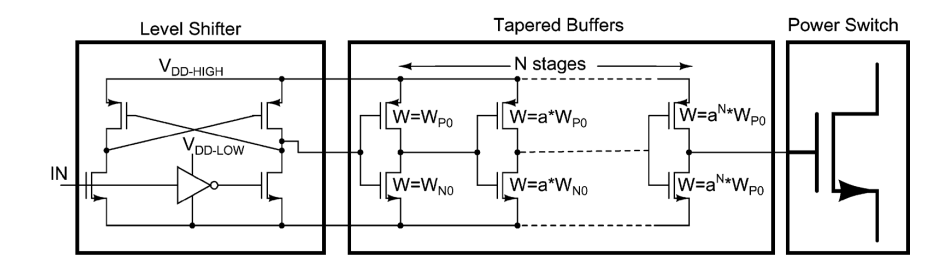


### Power Stage

Design of the power stage consists of sizing of the PMOS and NMOS, and layout in a common centroid configuration that includes the current sensing FET. The size of the nmos and pmos will depend on die area and the target output power.

### Gate Drive Buffers

The gate drive buffers are a series of cascaded inverters, sized for optimal rise and fall time. [6] provides details on the correct design methodology, figure from [6] copied below. However, if we use the 5V logic cells we do not need to use the shown level shifting cell.



### Switch Control and Deadtime Generation

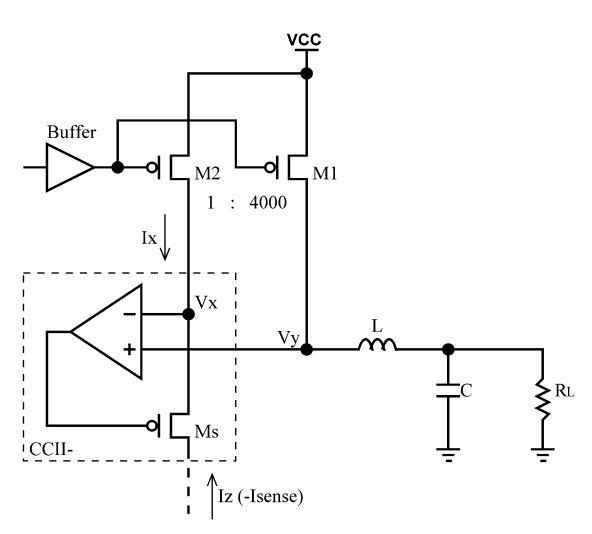
The modulator generates a signal determining if the pmos or nmos should be on. However, circuity is needed to generate non-overlapping signals for the two switches. The switch control module will generate adjustable deadtime using chains of logic gates from the SKY130 sky130\_fd\_sc\_hvl - High Voltage (5V) logic library. The switch control module interfaces with the SPI bus, which allows the deadtime to be controlled and the switch state to be manually controlled if needed, both of which are important for verifying portions of the chip and for bringup.

Delays using logic gates are not constant over PVT variations, but they will relatively track the actually required deadtime.

This block also generates the blanking signal, which feeds back into the modulator.

### Current Sense Circuitry

We plan to implement the current sense circuit from [2] (shown below). This current sense circuit uses a feedback network to keep the current in a matched PMOS proportional to the current in the power PMOS. This requires an opamp with an input common mode range that extends to the positive supply and an output voltage that comes within |Vtp| of the positive supply. This can be achieved by the folded cascode opamp that is one of our functional units.



### Bias Generation

The bias generation block generates the cascode bias voltages and mirrors the off-chip pmos and nmos bias supplies, distributing these to the other analog blocks.

Single off-chip bias current is supplied. This is distributed to pmos and nmos current mirrors

### Digital Control Interface

The digital control interface is a SPI slave device which exposes a set of configuration registers to external devices, to be used during bringup and testing. Additional uses for configuration registers may arise during the design of the chip, but the initial design plan is to only use this block to for configuration of the switch control and Deatime generation block.

### Functional Unit - Folded Cascode Opamp

Folded cascode Opamp

Bandwidth: TBD

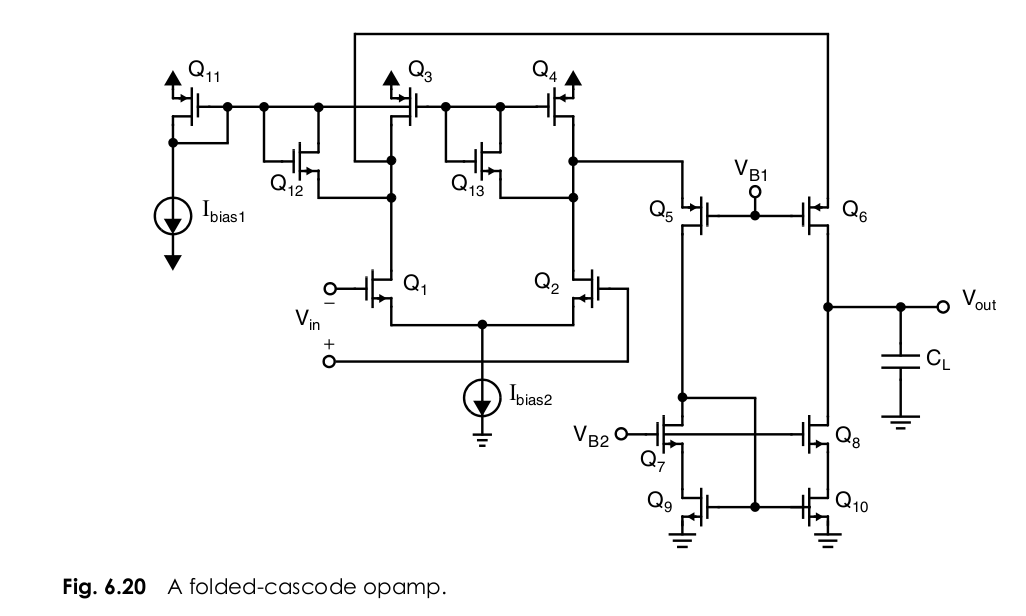
Vcm\_min: Vss + 2\* Vsat + Vtn = ~ 1.3V

Vcm\_max: Vdd-Vd\_sat+ Vtn

Vout\_min: 2\* Vsat

Vout\_Max: Vdd - 2\*Vsat

Schematic from [5]



### Functional Block - Comparator

Topology tbd

Input common mode range depends on current sense + offset from slope compensation, ideally low (Vss? Vss+ Vsat+Vtn?)

Propagation delay < 100ns

Offset not critical (<30mV?)

Needs hysteresis

## Pin List

| Name | Function | Functional Group |
| --- | --- | --- |
| Vdd Power (x2) | Power for power stage | Power |
| Gnd Power (x2) | Power for power stage | Power |
| SW Power (x2) | Switching node | Power |
| Vdd Analog | Lower noise supply for analog | Power |
| Gnd Analog (x2) | Lower noise supply for analog | Power |
| I\_PMOS | Current for PMOS current mirros | Bias |
| I\_NMOS | Current for NMOS current mirrors | Bias |
| I\_FREQ | Current to set switching frequency | Control |
| I\_COMP | Current to set compensation ramp | Control |
| VREF | Reference voltage for error amp | Control |
| Enable | System enable | Control |
| Vfeedback | Divided output voltage for error amp | Control |
| SPI\_CS | SPI Bus | Communication |
| SPI\_MOSI | SPI Bus | Communication |
| SPI\_MISO | SPI Bus | Communication |
| SPI\_CLK | SPI Bus | Communication |
| Vcomp | Compensation Pin | Monitoring / control |
| Isense | Voltage proportional to sensed current | Monitoring |
| Cycle End | Timing signal, end of switching cycle | Monitoring |
| Cycle Start | Timing cycle, start of switching cycle | Monitoring |

Total: 24 pins

If extra pins, can break out temperature monitoring diode, extra control signals

## Test Plan

Overriding the switching states via the registers controlling the switch control block allows almost every unit to be tested in isolation

### Current sensing test

Via the SPI interface, hold the PMOS to the on state. Then sink a known current from the switching node pin and measure the sensed current as output by the current sensing circuitry. Measure DC accuracy, transient response, and gain/phase.

### Error Amplifier tests

Drive the two inputs of the error amplifier and measure the response via the compensation pin. Measure gain/phase and offset voltage

### Switching Test

Sweep deadtime set points.

Measure switching time, measure switching current, ensure no overlapping of PMOS and NMOS conduction, calculate switching losses from measured data.

### System level tests

-Measure efficiency

-measure transient response

## Timeline

**March - April 3rd (first week of class):**

Finish “Gold model” of analog design

Review analog design with Prof. Boris Murmann

Finalize architecture decision for comparator

**April 4th - April 18th (first two weeks of april)**

Schematic capture and simulation of all blocks

Begin system level simulation

Write verilog for SPI interface

**April 19 - April 25th**

Validate system level simulation

Begin layout of blocks

**April 25- May 2**

Finish layout of blocks

Floorplan design

**May 2 - May 9**

Layout full design

**May 9 - May 16**

Layout full design

LVS and parasitic extraction

**May 16 - 23**

Post-route simulation

Design verification

**May 23-**

Slack for missed deadlines

**June 4th**

Tapeout

## Work Division

**Weston**

* Folded cascode opamp design
  + Error amplifier
  + Current sensing circuit
* Power stage
* Gate drive buffers
* Switch control and deadtime generation

**Aparna**

* Comparator
  + Oscillator
  + Modulator and slope compensation

**Both**

* Digital SPI interface
* Bias circuit

## Works Cited

[1]Texas Instruments. 2007. “Understanding and Applying Current-Mode Control Theory.” TI Application Notes. <https://www.ti.com.cn/cn/lit/an/snva555/snva555.pdf>.

[2] F. Ma, W. Chen and J. Wu, "A Monolithic Current-Mode Buck Converter With Advanced Control and Protection Circuits," in IEEE Transactions on Power Electronics, vol. 22, no. 5, pp. 1836-1846, Sept. 2007, doi: 10.1109/TPEL.2007.904237.

[3] Chi Yat Leung, P. K. T. Mok, Ka Nang Leung and M. Chan, "An integrated CMOS current-sensing circuit for low-Voltage current-mode buck regulator," in IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 52, no. 7, pp. 394-397, July 2005, doi: 10.1109/TCSII.2005.850403.

[4] STM32H725 Datasheet <https://www.st.com/resource/en/datasheet/stm32h725ae.pdf>

[5] Carusone, T. C., Martin, K. W., & Johns, D. (2011). *Analog integrated circuit design, 2nd edition*. Hoboken, NJ: John Wiley & Sons.

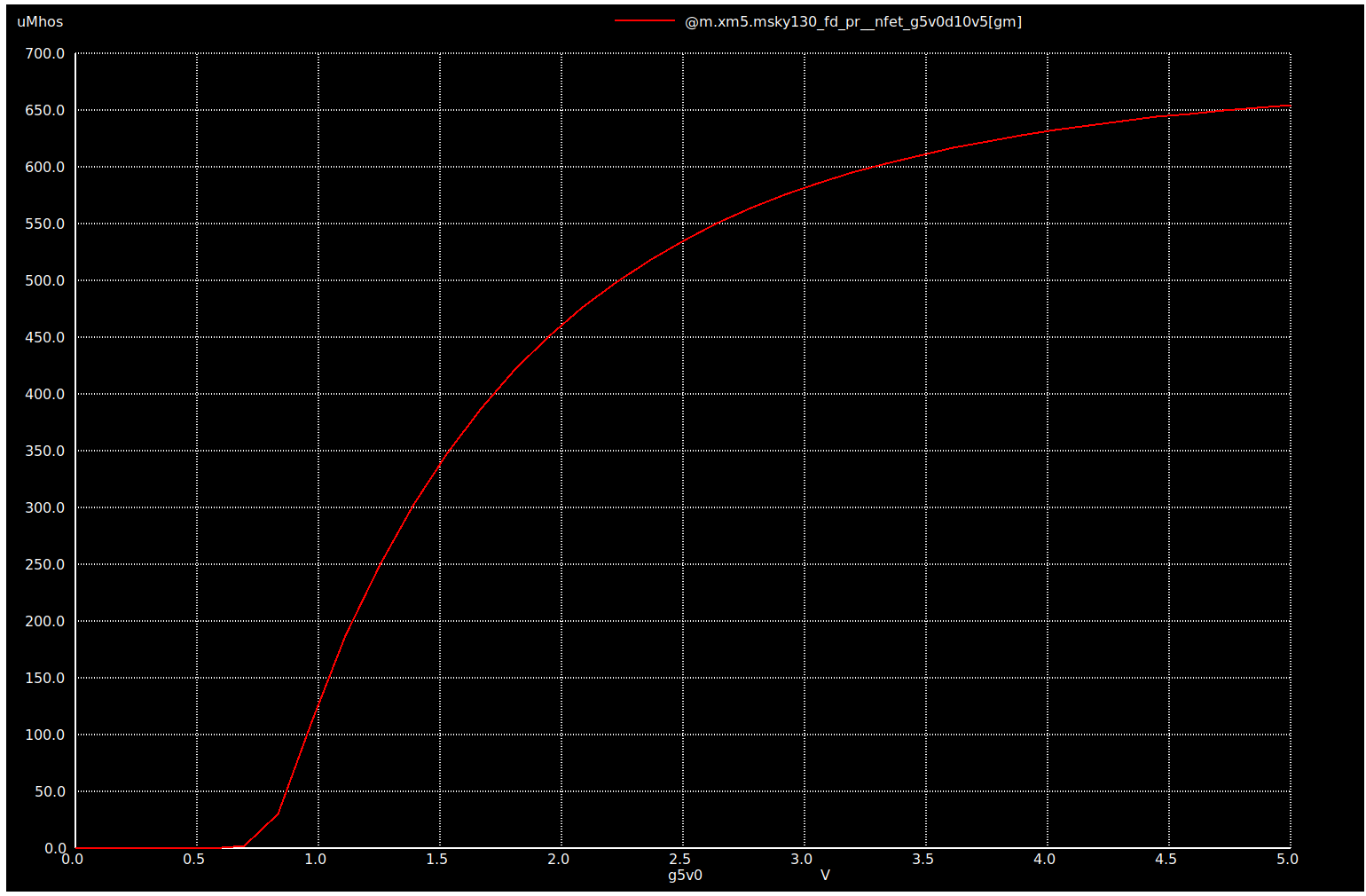
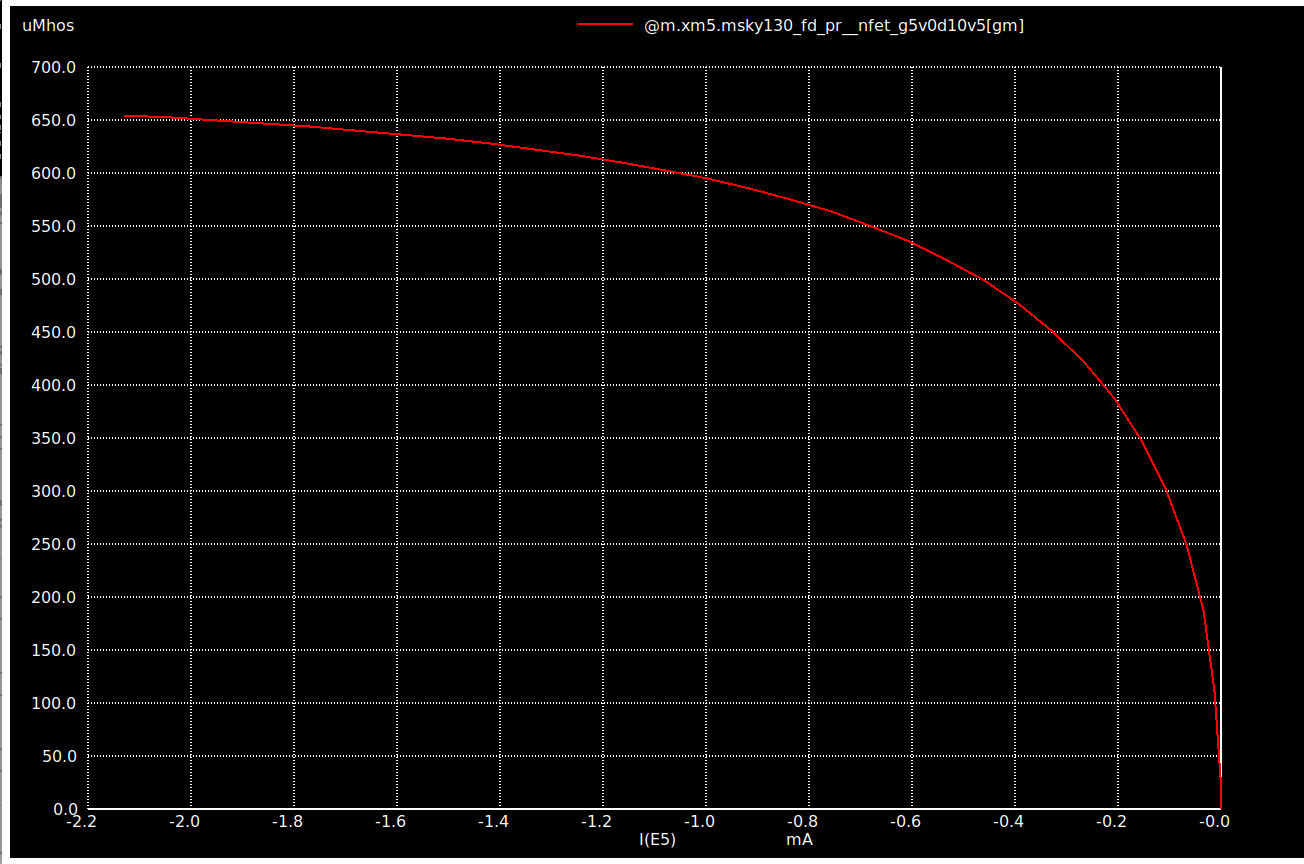
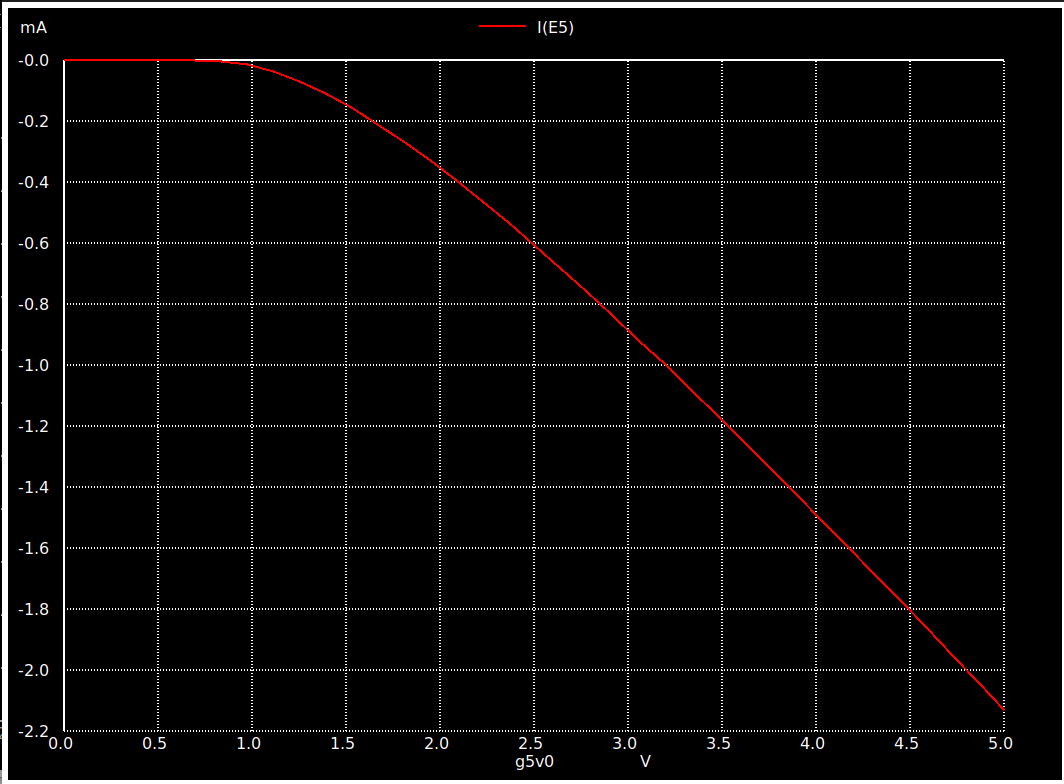
[6] R. C. N. Pilawa-Podgurski and D. J. Perreault, "Merged Two-Stage Power Converter With Soft Charging Switched-Capacitor Stage in 180 nm CMOS," in IEEE Journal of Solid-State Circuits, vol. 47, no. 7, pp. 1557-1567, July 2012, doi: 10.1109/JSSC.2012.2191325.

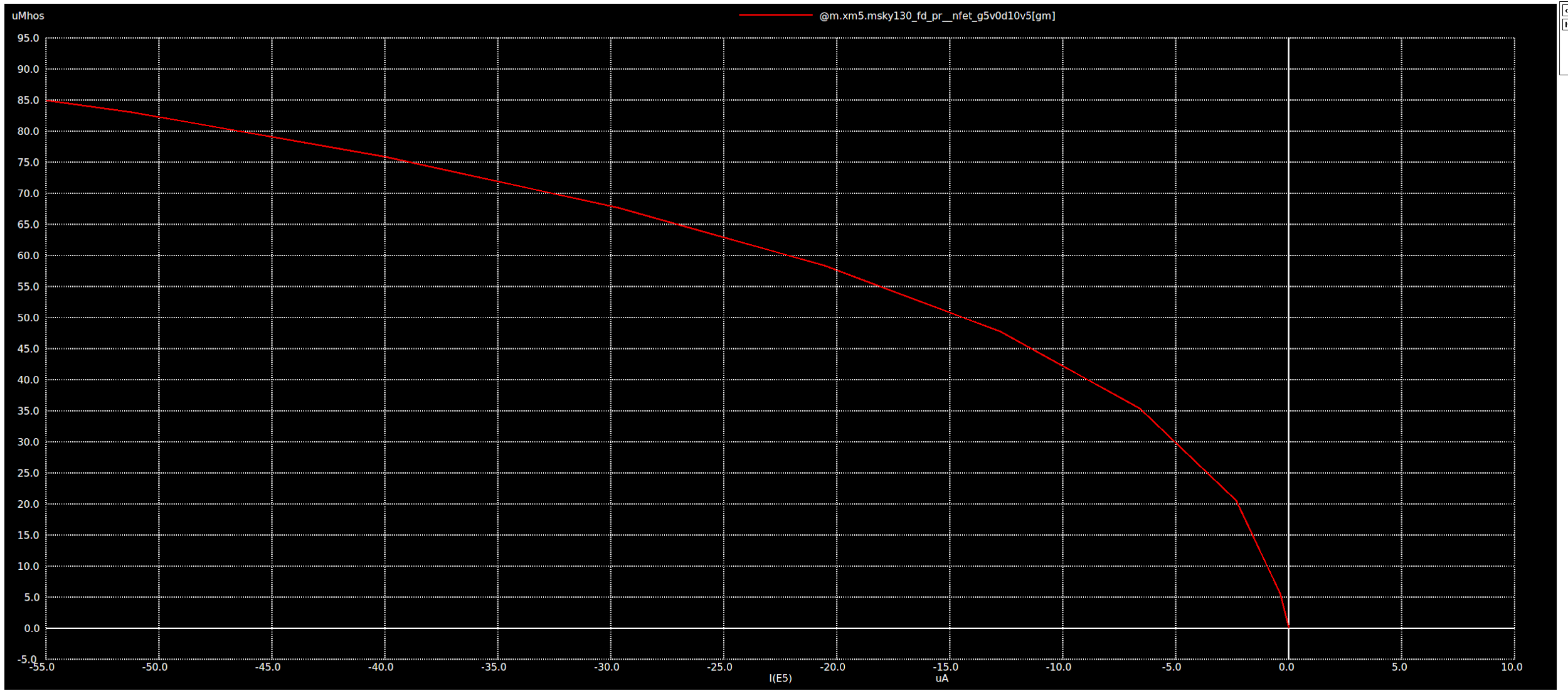
## Design Work

### Transistor Sizing

Due to supply voltages, all transistors in the design will be nfet\_g5v0d10v5 and pfet\_g5v0d10v5. No exhaustive search, but 1um width seems like a good compromise between minimum channel size and maintaining decent Ro.

Plots of 5/1 nmos:





### Questions for 4/12 Boris meeting:

**Compensation**

* **Clamping circuit for Vcomp**

**Slope Compensation / Oscillator**

* **How low can current source go / how large can capacitor go**
* **200nA?**

**Bias Sources**

* **How large should off chip current sources be. Filtering?**

**Verification**

* **How should we model parasitics of power section**
* **What corners should we check / monte carlo simulation**

**Layout**

* **How to lay out, what should modular blocks be?**

**Power Stage**

* **Rough value on on resistance vs interconnect**
* **How should we model switch for verification**
* **How to lay out driver stages**

**Debug Signals**

* **Current mirror with TIA on PCB?**

**Bringup**

* **Use 128 bit LA bus to trim any current sources or anything?**

Clamping circuit for Vcomp / setting maximum current limit

Magnitude of current source for biasing

Filtering of current source from off chip

How to modularize layout

Layout of power FET / calculating SOA

* How to lay out pre-drivers